53. (Amended) The programmable input/output device of claim 52 wherein the differential logic standard is a standard selected from the group consisting of HSTL and GTL.

54. (Amended) The programmable input/output device of claim 52 wherein the first logic standard is a standard selected from the group consisting of TTL or CMOS.

55. (Amended) The programmable input/output device of claim 52 wherein the programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, and antifuse elements.

62. (Amended) A programmable input/output buffer capable of operating at multiple logic standards comprising:

an input/output terminal;

a plurality of programmable elements; and

[an input buffer; and]

an output buffer having circuitry controlled by at least one of the plurality of programmable elements to select between one logic standard and a differential logic standard.

63. (Amended) The programmable input/output device of claim 62 wherein the differential logic standard is a standard selected from the group consisting of HSTL and GTL.

64. (Amended) The programmable input/output device of claim 62 wherein the first logic standard is a standard selected from the group consisting of TTL and CMOS.

65. (Amended) The programmable input/output device of claim 62 wherein the programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, and antifuse elements.

67. (Amended) The programmable input/output device of claim 62 further comprising an [intput] input buffer having circuitry controlled by at least one of the plurality of programmable elements to select between the first logic standard and the second logic standard.

72. (Amended) The programmable input/output device of claim 71 wherein the input buffer and the output buffer further comprise means for modifying signals applied to the input/output